Restrict AGC & DC offset

WHAT IS CLAIMED IS:

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1. A feedback loop circuit apparatus for reducing DC offset in a communication channel, comprising:

a summing node in a receiver channel, wherein a receiver channel signal is coupled as an first input to said summing node; and

an integrator that has an input coupled to a second node of said receiver channel, wherein an output of said integrator is coupled as a second input to said summing node.

2. The apparatus of claim 1, wherein the communication channel is a wireless local area network (WLAN) receiver channel.

3. The apparatus of claim 1, wherein said integrator has a frequency response that is varied to vary a frequency response of the receiver channel.

4. The apparatus of claim 3, wherein said integrator frequency response is controlled to vary the frequency response of the feedback loop circuit to a first frequency response, a second frequency response, and a third frequency response each having a corresponding lower 3 dB frequency, wherein said first frequency response has a relatively low lower 3 dB frequency, said second frequency response has a relatively medium lower 3 dB frequency, and said third frequency response has a relatively greater lower 3 dB frequency.

5. The apparatus of claim 1, wherein said integrator includes an amplifier, a capacitor, and a resistor arranged in an integrating amplifier configuration.

6. The apparatus of claim 1, wherein said integrator includes an amplifier, a

capacitor, and a variable resistor arranged in an integrating amplifier configuration.

7. The apparatus of claim 6, wherein said variable resistor is varied to alter the frequency response of said integrator.

8. The apparatus of claim 7, wherein said variable resistor includes:
at least one resistor; and
at least one switch across said at least one resistor.

9. The apparatus of claim 7, wherein said variable resistor includes:
a first resistor;
a second resistor coupled in series with said first resistor;
a first switch coupled across said second resistor;
a third resistor coupled in series with said second resistor; and
a second switch coupled across said third resistor.

10. The apparatus of claim 9, wherein said first switch receives a first control signal, and said second switch receives a second control signal, wherein said first and second control signals are sequenced in three consecutive time periods according to the following table:

	first control signal	second control signal
first time period	1	1
second time period	0	1
third time period	0	0

11. The apparatus of claim 10, wherein said third resistor has a larger resistance

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value than said second resistor, and wherein said second resistor has a larger resistance value than said first resistor.

12. The apparatus of claim 10, wherein said first time period is within the range of 5 to 6 microseconds, and wherein said second time period is within the range of 55 to 128 microseconds.

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13. The apparatus of claim 1, wherein said integrator is configured in an inverting integrator configuration.

14. The apparatus of claim 1, further comprising:

at least one amplifier that couples said second node to said input of said integrator.

15. The apparatus of claim 14, wherein said amplifier is configured as a differential amplifier.

16. The apparatus of claim 1, wherein said receiver channel signal is a radio frequency signal.

17. The apparatus of claim 1, wherein said receiver channel signal is an intermediate frequency signal.

18. An apparatus for gain control in a communication channel, comprising:

a multiplier that receives a first automatic gain control (AGC) signal and outputs a second AGC signal;

a first AGC amplifier that receives said first AGC signal; and

a second AGC amplifier that receives said second AGC signal.

19. The apparatus of claim 18, wherein the communication channel is a wireless local area network (WLAN) receiver channel.

20. The apparatus of claim 18, wherein said second AGC amplifier is located upstream in a receiver channel from the first AGC amplifier.

21. The apparatus of claim 18, wherein said second AGC amplifier receives a radio frequency signal and said first AGC amplifier receives a baseband signal.

22. The apparatus of claim 18, wherein said second AGC amplifier receives a radio frequency signal and said first AGC amplifier receives an intermediate frequency signal.

23. The apparatus of claim 18, wherein said multiplier multiplies said first AGC signal by an integer amount to generate said second AGC signal.

24. The apparatus of claim 23, wherein said multiplier multiplies said first AGC signal by an integer amount, and said integer amount is equal to 2.

25. The apparatus of claim 18, wherein said multiplier comprises an operational amplifier.

26. A method for reducing DC offset in a communication channel, comprising the steps of:

(1) integrating an output signal available at a first node to generate an integrated signal; and

(2) summing the integrated signal with a receiver channel signal at a second node, wherein the first node is downstream from the second node in a receiver

channel.

27. The method of claim 26, wherein the communication channel is a wireless local area network (WLAN) receiver channel.

28. The method of claim 26, wherein step (1) includes the step of:

generating the integrated signal as an integrated and inverted version of the output signal.

29. The method of claim 26, wherein step (1) is performed by an integrator circuit, wherein the integrator circuit includes an amplifier, a capacitor, and a resistor, the method further comprising the step of:

arranging the amplifier, capacitor, and resistor in an integrating amplifier configuration.

30. The method of claim 26, wherein said step (1) is performed by an integrator circuit, the method further comprising the step of:

(a) varying the frequency response of the integrator circuit in response to a control signal.

31. The method of claim 30, wherein the integrator circuit includes an amplifier, a capacitor, and a variable resistor, the method further comprising the step of:

arranging the amplifier, capacitor, and variable resistor in an integrating amplifier configuration.

32. The method of claim 31, wherein step (a) comprises the step of:

varying the value of the variable resistor to alter the frequency response of the integrator circuit.

33. The method of claim 32, further comprising the step of:

(i) configuring the variable resistor.

34. The method of claim 33, wherein the variable resistor includes at least one resistor and at least one switch, step (i) comprising the step of:

coupling said at least one switch across said at least one resistor.

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35. The method of claim 33, wherein the variable resistor includes a first resistor, a first switch, a second resistor, a second switch, and a third resistor, step (i) comprising the steps of:

coupling the first switch across the second resistor;

coupling the second resistor in series with the first resistor;

coupling the second switch across the third resistor; and

coupling the third resistor in series with the second resistor.

36. The method of claim 35, further comprising the steps of:

(I) receiving a first control signal with the first switch;

(II) receiving a second control signal with the second switch; and

(III) sequencing the first and second control signals according to the following table:

	first control signal	second control signal
first time period	1	1
second time period	0	1
third time period	0	0

37. The method of claim 36, wherein step (III) comprises the step of:

sequencing the first and second control signals, wherein the first time period is in the range of 4 to 6 microseconds, and wherein the second time period is in the range of 55 to 128 microseconds.

38. The method of claim 36, further comprising the steps of:

receiving a data frame preamble during the first and second time periods; and

receiving a data portion of the data frame corresponding to the preamble during the third time period.

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39. The method of claim 26, wherein step (2) comprises the step of:

receiving the receiver channel signal, wherein the receiver channel signal is a radio frequency signal.

40. The method of claim 26, wherein step (2) comprises the step of:

receiving the receiver channel signal, wherein the receiver channel signal is an intermediate frequency signal.

41. A method for gain control in a communication channel, comprising the steps of:

(1) multiplying a first automatic gain control (AGC) signal by an amount to generate a second AGC signal;

(2) providing the first AGC signal to a AGC amplifier; and

(3) providing the second AGC signal to a second AGC amplifier.

42. The method of claim 41, wherein the communication channel is a wireless local area network (WLAN) receiver channel.

43. The method of claim 41, further comprising the step of:

positioning the second AGC amplifier upstream in a receiver channel from the first AGC amplifier.

44. The method of claim 43, further comprising the steps of:

receiving a radio frequency receiver channel signal with the second AGC amplifier; and

receiving a baseband receiver channel signal with the first AGC amplifier.

45. The method of claim 43, further comprising the steps of:

receiving a radio frequency receiver channel signal with the second AGC amplifier; and

receiving an intermediate frequency receiver channel signal with the first AGC amplifier.

46. The method of claim 41, wherein step (1) comprises the step of:

multiplying the first AGC signal by an integer amount to generate the second AGC signal.

47. The method of claim 41, wherein step (1) comprises the step of:

multiplying the first AGC signal by 2 to generate the second AGC signal.

48. The method of claim 41, wherein step (1) comprises the step of:

amplifying the first AGC signal to generate the second AGC signal.

49. A method for reducing DC offset in a communication channel, comprising the steps of:

(1) measuring a DC offset voltage present in an output signal at a first node; and

(2) removing the measured DC offset voltage from a receiver channel signal at a second node, wherein the first node is downstream from the second node in a receiver channel.

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50. The method of claim 49, wherein step (1) comprises the step of:

integrating the output signal available at the first node to generate an integrated signal that includes the DC offset voltage.

51. The method of claim 50, wherein step (2) comprises the step of:

subtracting the integrated signal from the receiver channel signal at the second node.

52. The method of claim 49, wherein the communication channel is a wireless local area network (WLAN) receiver channel.

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